Version: 1.2 April 2000

Configuring IPM16 for 4:2:2:4 to 4:4:4:4 Conversion From a 601 Stream

Introduction

The IPM16 is a systolic image processing array capable of performing various operations on digital video and digital images. This application note describes the interpolation of 4:2:2:4 (YC_BC_R encoded) to 4:4:4:4 format. A portion of the processing array of the IPM16 will be configured as an interpolation filter. Figure 1 below illustrates the block diagram for this function.

Overview

The filter size specification and filter coefficients are preloaded into IPM16. Luma, multiplexed chroma, and alpha channels enter the input interface at a 1x pixel clock rate (see Figure 3 on back) where the H and V timing signals are generated and the data is processed into the IPM16 internal data format. Blank, Pixel, Line, and Field (BPLF) are derived from H and V to provide control signals for the filter. In the processing array, the multiplexed chroma is interpolated at a 2x pixel clock rate (see Figure 3 on back) by a symmetric lowpass filter. The filter can be designed to achieve higher efficiency by folding. Luma, alpha channel, and ancillary data streams bypass the interpolation filter and are re-equalized to the video stream at the output interface. Other processes, such as color space conversions, keying, filtering, blending, etc., can be performed as well. The output interface performs clipping and conditioning on data and inserts sync onto the stream if needed. The IPM16 outputs 4:4:4:4 data at 1x pixel clock rate.

Edge Processing, H and V Timing

The SAV and EAV embedded codes of the ITU-601 compliant data are processed at the input interface to generate H and V timing signals. For internal reference, the control signals are passed along with the data. The transition between blanking and active video is processed to reduce high-frequency components that could cause ringing.

Numeric Format

The IPM16 numeric formats have higher precisions than the original 8 bit or 10 bit 4:2:2:4 data. Padding / rounding are performed at the input / output interfaces as needed for the numeric format conversion. During the internal process, the data always retains its 16 bit precision.

Interpolation Filter

The interpolation filter is comprised of three parts:

- Delay units allowing for multiple taps
- Multipliers that compute intermediate results from pixel values and filter coefficients
- The summation unit for summing intermediate results

The total amount of delay is determined by filter size.

Block Diagram

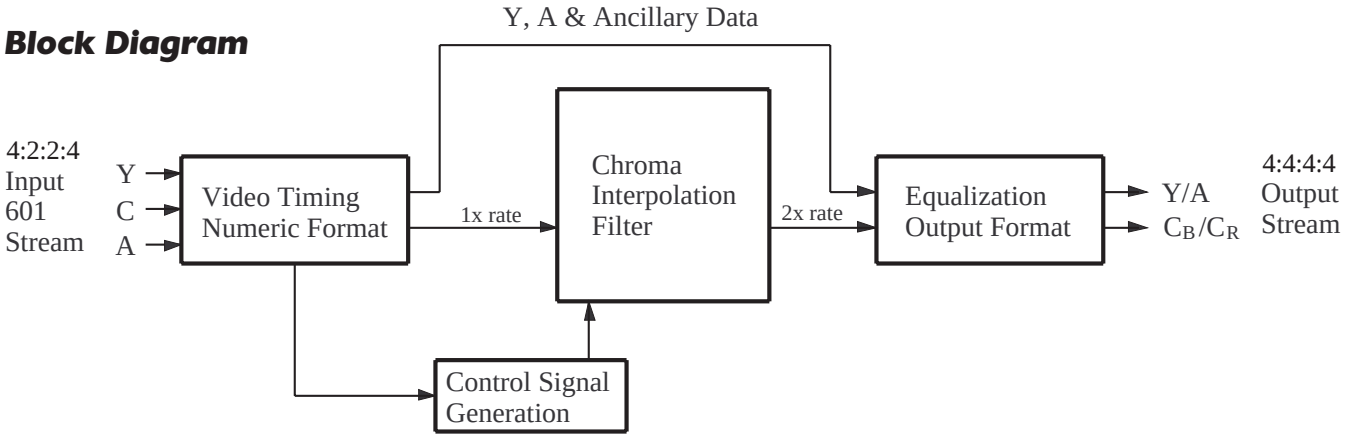

Figure 1: Block Diagram for 4:2:2:4 to 4:4:4:4 Format Conversion

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Folding and Filter Efficiency

For symmetric filters, folding is used to reduce the number of multipliers used in the processing array. As shown in Figure 2 below, two pixel values to be multiplied by the same coefficient are brought together by folding the connection of delay units. These two pixels are added before multiplication is performed in the arithmetic units.

Besides folding, the arithmetic units perform multiplications at 2x clock rate. C_B and C_R are computed on even and odd phases of a 1x clock to increase filter efficiency.

I/O Streams

Luma, multiplexed chroma, and alpha channel enter the IPM16 at 1x clock rate. H and P are generated for timing and control. Outputs are time-division multiplexed streams. The 1x 4:4:4:4 stream may be output by two time-division multiplexed streams running at 2x rate, or alternatively by a single time-division multiplexed stream running at 4x rate. Interpolated new data values are shaded in Figure 3 below.

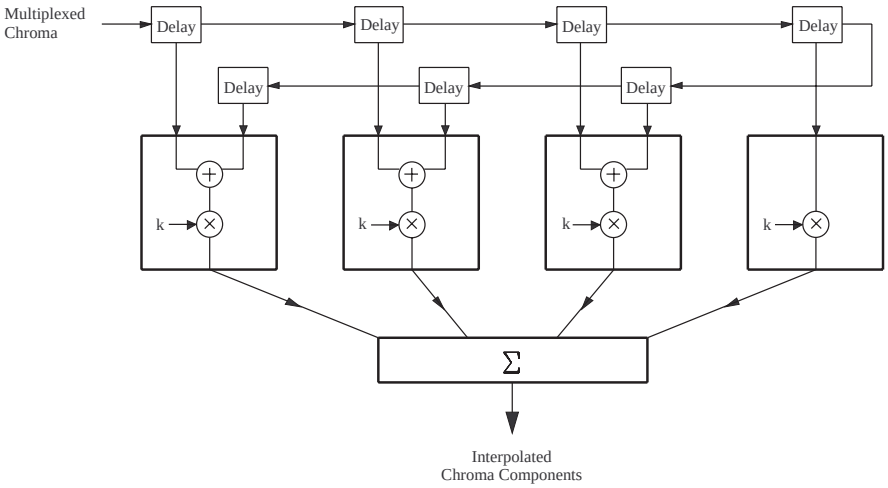

Figure 2:
Filter folding – K represents the coefficient

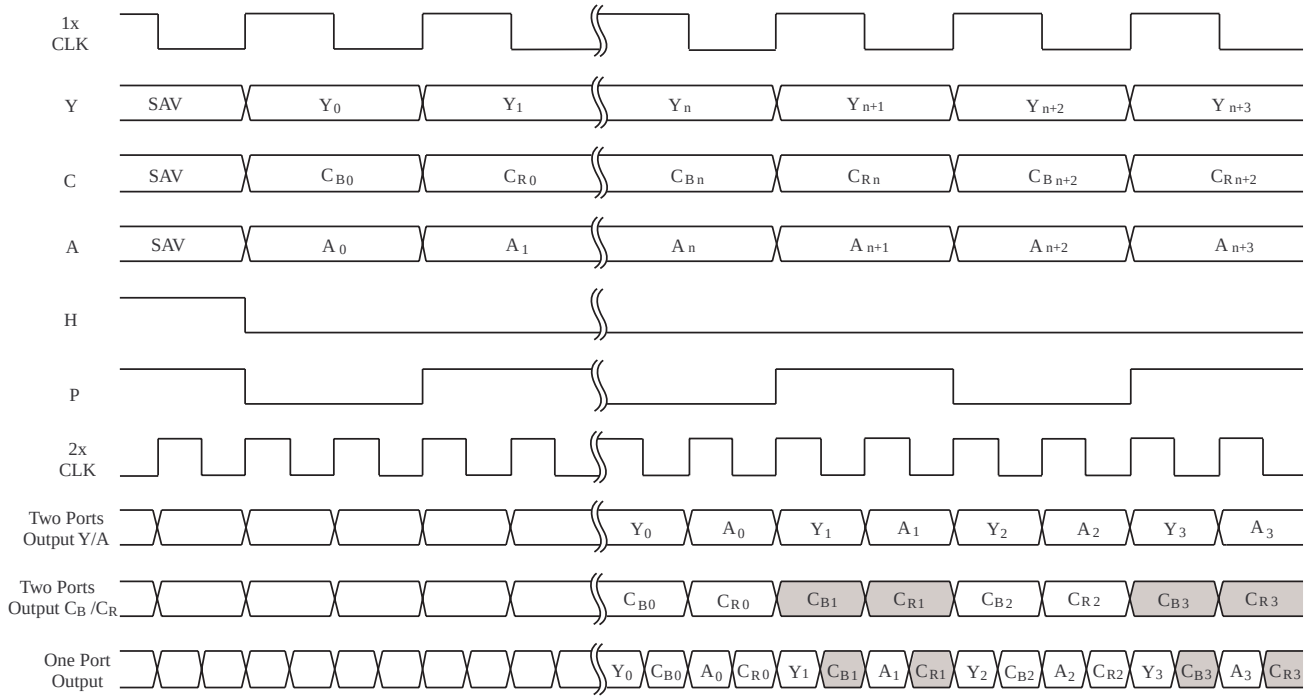

Figure 3: Data streams and control signals in the conversion process
(Shaded areas indicate new interpolated values.)

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