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Configuring IPM16 For 2-Dimensional Filtering

Introduction

The IPM16 is a systolic image processing array capable of performing various operations on digital video and digital images. This application note describes 2-dimensional filtering on a YC_BC_R encoded 4:4:4:4 stream using an IPM16 with an external FIFO. The FIFO provides multiple line delays for vertical filtering. The IPM16 is configured to process multiple lines with a convolution filter to reduce noise in a component video stream. Figure 1 below shows the block diagram for the 2-dimensional filtering process.

Overview

The filter size specification and filter coefficients are preloaded into an IPM16. Blank, Pixel, Line, and Field (BPLF) are derived from H and V to provide control signals. The 4:4:4:4 stream is pre-processed to the IPM16 internal format at the input interface. The external FIFO takes unfiltered 4:4:4:4 stream, produces line delays, and sends data back to the IPM16. Luma and chroma components of multiple lines are processed with a symmetric filter in the IPM16. The filter can be designed to achieve higher efficiency by folding and by operations at twice the data rate. Alpha channel and ancillary data streams bypass the processing unit and are re-equalized to the video stream at the output interface where clipping and output format conversions are also performed.

Line Delay FIFO

An external FIFO is used to provide multiple line delays. Data from one of the output sources is fed into the FIFO and recovered one (or more) line(s) later at the input interface. Delayed data from the FIFO is then routed to the arithmetic array for processing.

2-Dimensional Filter

A 2-dimensional filter takes multiple lines and outputs a filtered data stream. The filter is comprised of three parts:

- delay units allowing for multiple taps
- multipliers that compute intermediate results from pixel values and filter coefficients
- the summation unit for summing intermediate results

The total amount of delay is determined by filter size.

Numeric Format

The IPM16's numeric formats have higher precisions than the 8 bit or 10 bit 4:4:4:4 data. Padding/rounding are performed at the input/output interfaces as needed for the numeric format conversion. During the internal process, the data always retains 16 bit precision.

Block Diagram

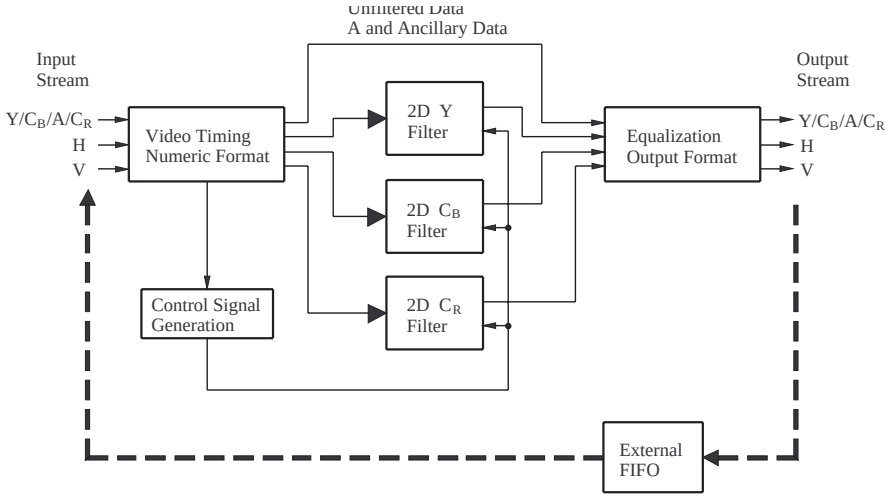

Figure 1: Block Diagram for 2 dimensional filters

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10050 N. Wolfe Road, SW2-152 • Cupertino, CA U.S.A. 95014-2528 • Tel: 408-725-3810 • Fax: 408-725-3819

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Folding and Filter Efficiency

For a fully symmetric filter, folding can be performed in either a horizontal or vertical direction to reduce the number of multiplications in the processing array. An example of horizontal folding can be found in Application Note 1 "Configuring IPM16 for 4:2:2:4 to 4:4:4:4 Conversion From a 601 Stream". Figure 2 below shows an example of vertical folding. Current and delayed pixels are added together and multiplied by a single coefficient in an arithmetic unit.

Besides folding, the arithmetic units compute two intermediate values every pixel clock to increase filter efficiency. Filtered data values are obtained by adding even and odd phases of a pixel clock.

Edge Processing, H and V Timing

The H and V signals are used to provide internal reference and output timing. The transition between blanking and active video is processed to reduce high-frequency components that could cause ringing.

I/O Streams

The 4:4:4:4 time-division multiplexed data arrives at the input interface every 1x pixel clock. Each component, in the order of Y, C_B, A, and C_R, occupies a quarter of a 1x pixel clock. Four 1x data streams are recovered by the input interface for further processing. The "intermediate Y" shown in Figure 3 below represents a 1x data stream used by a filter. At the output interface a 1x filtered data stream is produced in the time-division multiplexed format.

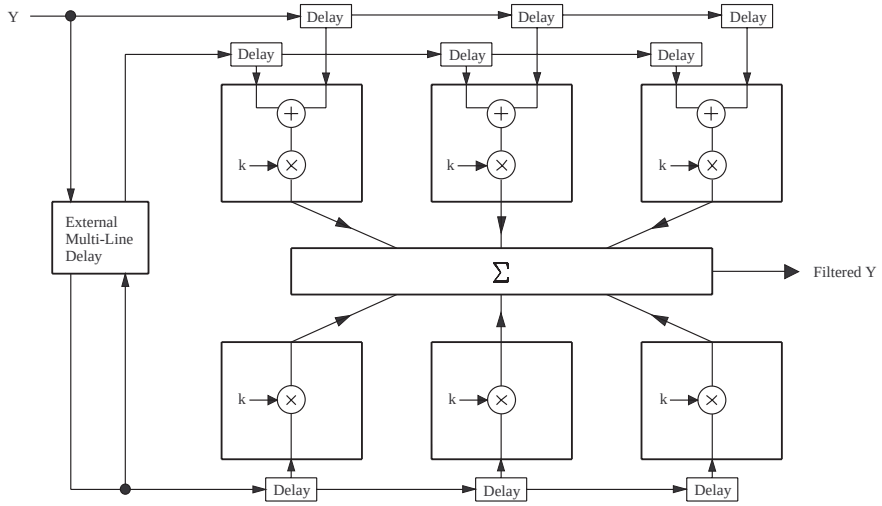

Figure 2: Folding in vertical direction, k represents the coefficient

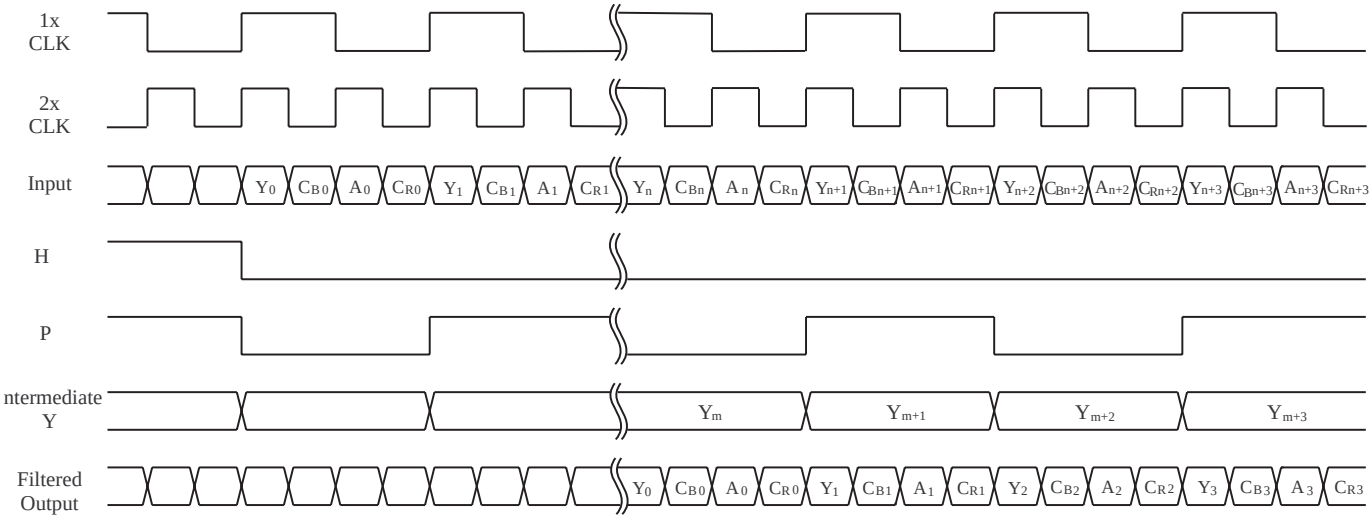

Figure 3: Data streams and control signals in the filtering process

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