Version: 1.1 April 1999

Configurable Systolic Image Processing Array

Features

- **Real-time systolic operation**
  - up to 240 MSamples/sec
- **Internal 16 bit per component precision**
- **Variable pixel clock up to 80 MHz**
- **Preserves ancillary data**
- **Arithmetic level reconfigurable computing**
  - add, subtract, multiply, compare, min, max, abs
  - combine mathematical operations into complex algorithms
- **Allows for rapid product prototyping/production**
- **Supported scan rates:**
  - Interlace (PAL, NTSC)
  - Progressive
  - HDTV (Production/ATSC)
  - Film (up to 1920x1556)
- **Formats:**
  - Component (RGB, YIQ, YUV, Ycc, Y/C)
  - Composite
  - Key, Matte, Alpha support
- **Pixel Aspect Ratio**
  - Variable (including ITU-601 and square pixel)
- **Cascadable for increased processing power**
- **Image statistics support:**
  - mean, minimum, maximum, variance, std. deviation
- **Automatic delay compensation for internal processing**
- **Genlock for synchronizing to input or reference signals**

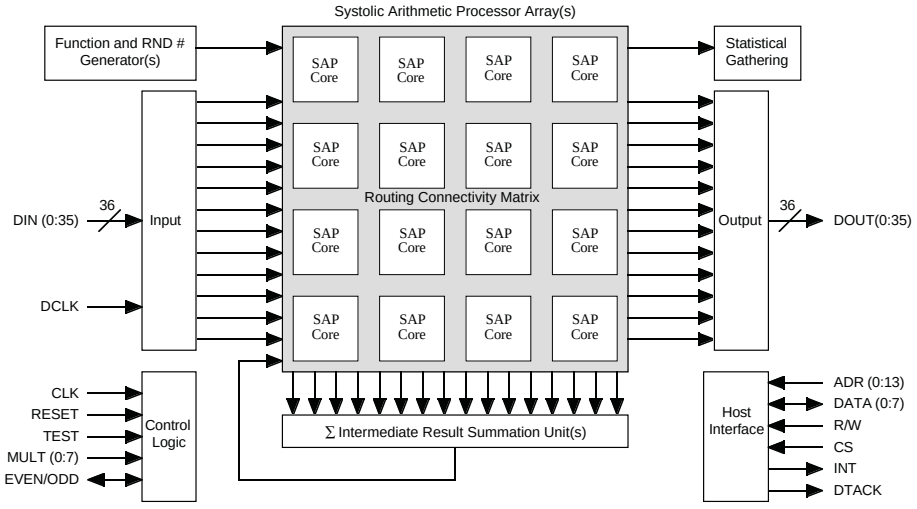
Device Description

The IPM16 is a new systolic array processing architecture designed to be configurable to operate in real-time on video at an arithmetic level.

Real-Time Applications

- **MPEG/DCT artifact/Mosquito noise removal**
- **Colorspace conversion (RGB, YIQ, YUV, Ycc, etc.)**
- **Blending/overlay (station I.D., logo, "bug")**
- **Medical imaging processing**
- **Chroma keying/compositing**
- **Line doubling/quadrupling**
- **Group delay compensation**
- **Teleconferencing**
- **Image processing**
- **Video legalization**
- **HDTV equipment**
- **Set-top devices**
- **PC multimedia**
- **Filtering**
  - FIR
  - Pre- and post-compression
  - Noise reduction
  - Image enhancement
  - Interpolation/decimation
  - Adaptive comb

Block Diagram



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Overview

Arithmetic level reconfigurable computing

The IPM16 is the first device in a new class of MSIC™* media processors focused on video and image processing applications. While similar to an FPGA, the IPM16 is configurable at the arithmetic operation level (addition / subtraction / multiplication / comparison / min / max) rather than at the Boolean logic level (and / or / xor / invert). The IPM16's configurability permits consolidation of many previously dedicated ASIC functions, allowing the IPM16 to replace an existing chip or multiple chips in a design. Many different functions can be consolidated into a single IPM16, thus saving board space, reducing parts inventory, and increasing price / performance. For example, the IPM16 can take in a 4:2:2 ITU-601 video signal, interpolate to 4:4:4, colorspace convert to RGB, and then filter the RGB signal.

High-performance interface technology

The input and output interfaces have been designed to condition signals processed by the IPM16. Bit masking, rounding or padding, clipping, interpolation or decimation, and edge shaping or unshaping are allowed. Video synchronization information may be supplied with video signals; or it can be derived from ITU-601 data. For additional flexibility, the IPM16 can genlock to an input or reference signal. The data interfaces of the IPM16 allow for one or more concurrent signals, and provide support for a variety of format types. Time-division multiplexed I / O allows multiple video signals to pass through the IPM16 using only 36 input pins and 36 output pins. Support for 2D and 3D filtering is provided by an external FIFO or frame buffer.

Pin Descriptions

Signal	I/O	Description	Signal	I/O	Description
CLK	I	Master Clock	ADR (0:13)	I	Host Interface Address Bus
$\overline{\text{RESET}}$	I	Reset	DATA (0:7)	I / O	Host Interface Data Bus
$\overline{\text{TEST}}$	I	Test	R / $\overline{\text{W}}$	I	Host Interface Read / Write
DCLK	I	Data Clock (For DIN / DOUT)	$\overline{\text{CS}}$	I	Host Interface Chip Select
EVEN / $\overline{\text{ODD}}$	I / O	Data Even / Odd Flag	$\overline{\text{INT}}$	O	Host Interface Interrupt
DIN (0:35)	I	Data In (time-division multiplexed for multiple inputs)	DTACK	O	Host Interface Data Transfer Acknowledge
DOUT (0:35)	O	Data Out (time-division multiplexed for multiple outputs)	MULT (0:7)	I / O	GPI / Multipurpose / Genlock Signals

Ordering Information

Order Code	Package	Max Speed
IPM16	160 Pin PQFP	80 / 40 MHz

Samples available Fall 1999

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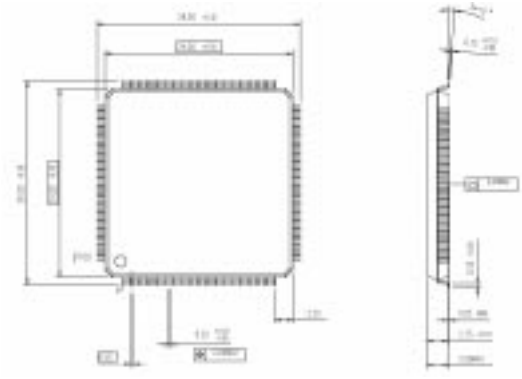
Package Dimensions



Actual Size

*(Market Specific Integrated Circuit) *MSIC is a trademark of Intelligent Paradigm, Inc.*